

REMARKS

Claims 1-36 were pending in the present application. Claims 4-5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27 and 29-36 are withdrawn from consideration. By virtue of this response, claims 1 and 22 have been amended, and new claims 37 and 38 have been added. Accordingly, claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28 and 37-38 are currently under consideration. Amendment and cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter of the claims as previously presented.

Rejections under 35 USC §112, ¶2

Claims 22, 24 and 28 are rejected as being indefinite. Applicant has amended these claims as suggested by the Examiner. It is submitted that, in any event, the scope of the claims before amendment is determinable by the Examiner. As such, it is submitted that the Examiner should have objected to the claims rather than rejecting the claims.

Claims 1-3, 6, 8 and 14 are rejected as being unpatentable under 35 USC §103(a) over Chang and Iwamatsu. Applicant respectfully traverses the rejection. In the first place, it is respectfully submitted that the combination of Chang and Iwamatsu fails to yield the subject matter of claim 1, and the dependent claims, as presently amended. In the second place, it is respectfully submitted, once again, that the combination of Chang and Iwamatsu is improperly made.

Chang and Iwamatsu each disclose a substrate or a substrate terminal is provided a predetermined voltage (116 in Figure 3 of Chang and VBG1 and VBG2, that is, CLK1 and CLK2 in Iwamatsu). The voltage is prepared in advance by the element side to change the reference value for element operation (threshold value for the gate) according to externally provided user data. The voltage is provided solely for reference value changing and is, for example, a DC voltage or a pulse.

In accordance with claim 1, a substrate terminal is provided with a signal representing “user data,” similarly to the gate terminal. Taking the example of Figure 2 of the present specification, a highly functional semiconductor element is constructed in a single MOSFET, in which the output goes HIGH only when the gate terminal input and the substrate terminal are both HIGH. Taking the example of Figure 3 of the present specification, a highly functional

semiconductor element is constructed in a single MOSFET, in which the output goes HIGH when at least either one of the gate terminal or the substrate terminal is HIGH.

Thus, for example, whereas conventional circuitry utilized four and six MOSFET's, respectively, to construct a NAND circuit and NOR circuit and an AND circuit and OR circuit, as described in the specification, according to the claimed subject matter, this circuitry can be constructed with only two MOSFET's. Thus, integration of the semiconductor device may be greatly improved.

While the above cited examples are not to be construed as limiting the claims, it can be seen that the combination of Chang and Iwamatsu do not disclose or suggest the use of a substrate terminal as a terminal to receive any given signal provided externally as user data, to make such integration of a semiconductor possible. This user data are not signals prepared in advance by the element side solely to raise the threshold value, as described in the references. Rather, the user data are signals representing any value.

While it is recognized that the particular term "user data" is not explicitly explained in the specification, it is respectfully submitted that the term, when taken in view of the specification and the conventional art, is impliedly included in the description as filed. For example, the inputs IN1 and IN2 are input signals which are not signals prepared in advance by the element side solely to raise the threshold value as in the references, but are signals to be provided externally (and, as shown in the conventional art) to accomplish logic circuits such as a 2-input to 1-output NAND circuit, with the substrate terminal and the gate terminal being fed with similar data and the two signals (IN1, IN2) play equal roles.

In addition to the combination of Chang and Iwamatsu not yielding the subject matter of the rejected claims, as amended, it is again submitted that the combination of Chang and Iwamatsu is improperly made. In particular, the Examiner states two interrelated reasons for making the combination.

First, in the body of the rejection, the Examiner states "It would have been obvious to have the electrical connections of Iwamatsu in Chang et al. because they create a CMOS level shifter circuit having a concise level shift and a low reduction in an integration degree. In addition, the electrical insulation layer [14] of Chang et al. insulates all the terminals of the PMOS, NMOS

and the wells.” Then, in the response to Applicant’s arguments of May 5, 2003, the Examiner states that “However, it is well known in the art that the semiconductor structure of Chang et al. is a well known CMOS device structure. The CMOS structure of Chang et al. can be used in any circuit that would require a CMOS device. Therefore, the CMOS structure of Chang et al. can be used in any circuit connection, including the circuit connection of Iwamatsu. Therefore, it is reasonable to combine the devices of Chang et al. and Iwamatsu.”

It is respectfully considered that the Examiner is using a prohibited “obvious to try” motivation. That is, the case law is clear that there must be some motivation, whether explicit or implicit, in the prior art or knowledge held by one of ordinary skill in the art, to make the combination. Here, the Examiner essentially concedes that there is no explicit motivation to make the combination. The Examiner relies on the Chang structure being “well known in the art” as the apparent motivation for using the Chang structure to accomplish the Iwamatsu circuit connection. In other words, the Examiner is contending that it would be “obvious to try” the combination.

What the Examiner fails to consider is that there are numerous well known CMOS device structures. The Examiner has not pointed to anything in the prior art that indicates particular parameters are critical or that indicates the particular choice of the Chang et al. CMOS device structure would yield a successful result for accomplishing the Iwamatsu circuit connection. At the very least, this is what would be required to support an obviousness rejection. See, for example, MPEP 2145, which provides guidance to Examiners on how to properly rebut an applicant’s “obvious to try” argument

MPEP 2145 references the In re O’Farrell case. In the O’Farrell case, the court held the claimed method obvious because one reference contained a detailed enabling methodology, a suggestion to modify the prior art to produce the claimed invention, and evidence suggesting the modification would be successful. Here, the Examiner has provided a reference that, even if it contains a detailed enabling methodology, does not include a suggestion to modify the prior art to produce the claimed invention. Nor, it follows, has the Examiner provided evidence suggesting that the modification would be successful.

In summary, then, it is respectfully submitted that the combination of Chang and Iwamatsu fails to yield the subject matter of the rejected claims, as amended. It is further respectfully submitted that the combination of Chang and Iwamatsu is, in any event, improperly made.

Allowed Claims 10, 12, 16, 18, 20 and 26

Applicant appreciates the Examiner's indication that claims 10, 12, 16, 18, 20 and 26 are allowable.

Claim 22, Allowable Subject Matter

Applicant appreciates the Examiner's indication that claim 22 is allowable if rewritten in independent form. Applicant has so rewritten claim 22.

New Claims

New claims 37 and 38 have been added, dependent on claim 1, to recite additional subject matter. It is respectfully submitted that these claims are fully supported by the application as filed and further, that this subject matter is patentable over the cited references.

CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no.247322001700. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

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